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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/635,079

08/06/2003

Richard W. Adkisson

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09/17/2007

HEWLETT PACKARD COMPANY

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INTELLECTUAL PROPERTY ADMINISTRATION

FORT COLLINS, CO 80527-2400

EXAMINER

TABONE JR, JOHN J

ART UNIT

PAPER NUMBER

2117

MAIL DATE

DELIVERY MODE

09/17/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/635,079

Applicant(s)

ADKISSON ET AL.

Examiner

John J. Tabone, Jr.

Art Unit

2117

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 08062007.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application
- ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 have been examined.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 08/06/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

3. The disclosure is objected to because of the following informalities: The blank lines in paragraphs [0002], [0003] and [0022] – [0022] must be filled in with the appropriate information or removed from the specification. Appropriate correction is required.

Claim Objections

4. Claims 19 and 20 are objected to because of the following informalities: Legal type language (thereof) should be remove form these claims. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 9, 18 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9:

This claim recites the limitation "S". There is insufficient antecedent basis for this limitation in the claim. It appears that this claim should depend on claim 8 not claim 1.

Claim 18:

This claim recites the limitation "S". There is insufficient antecedent basis for this limitation in the claim. It appears that this claim should depend on claim 17 not claim 10.

Claim 23:

This claim recites the limitation "*the control signal*". There is insufficient antecedent basis for this limitation in the claim. It appears that this claim should depend on claim 20 not claim 2.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims **1, 2, 4-7, 10, 11, 13-16, 19, 20, and 21** are rejected under 35 U.S.C. 102(b) as being anticipated by **Ranson et al.** (US-5887003), hereinafter Ranson.

Claims 1, 10 and 19:

Ranson teaches the method of **claim 19** and the zeroing circuit (**Fig. 12, programmable state machine entry**) to execute this method for a general purpose performance counter ("GPPC") (**Fig. 13, counters 0-3**) connected to a bus carrying debug data (**Figs. 11 and 12, state machine input bus 1110**). **Ranson** also teaches the zeroing circuit comprises logic for zeroing out a specified number of most significant bits ("MSBs") (**Fig. 12, OR 1218, AND 1220, exclusive OR 1221, AND 1222**) of a selected portion of the debug data (**Fig. 12, via element 1202 (bit-wise select)**) based on a mask generated by a mask generator block (**Fig. 12, storage element 1204 (bit-wise mask)**) and means for providing a selection control signal (**storage elements 1201-1210 would be loaded with data by writing to state machine/counters control register circuitry 346**) to the mask generator block (**storage element 1204**), the selection control signal operating to select the specified number of MSBs for zeroing. (Col. 15, l. 19 to col. 16, l. 49).

Claims 2, 11 and 21:

Ranson teaches the logic for zeroing out a specified number of MSBs comprises logic for ANDing the inverted value of each bit of the mask with a corresponding bit of the selected portion of the debug data (**Exclusive OR gate 1221 couples the output of AND gate 1220 to one of the inputs of AND gate 1222 as shown, and also provides a selectable inversion function**). (Col. 15, ll. 40-47).

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Claims 4 and 13:

Ranson teaches the mask generator block is implemented using a plurality of multiplexers (**Fig. 14, multiplexers 1408 provides a 3-bit bus**), the selection control signal operating to select inputs of each of the multiplexers. (Col. 15, l. 19 to col. 16, l. 49).

Claims 5 and 14:

Ranson teaches the logic for ANDing comprises an AND circuit (**Fig. 12, AND gates 1220, 1222**).

Claims 6 and 15:

Ranson teaches the AND circuit comprises a plurality of 2-input AND gates Fig. 12, AND gate 1220 with 11 bit input).

Claims 7 and 16:

Ranson teaches each of the 2-input AND gates comprises an inverter input connected to receive a bit of the mask and an input connected to receive a corresponding bit of the selected portion of the debug data (**Exclusive OR gate 1221 couples the output of AND gate 1220 to one of the inputs of AND gate 1222 as shown, and also provides a selectable inversion function**). (Col. 15, l. 19 to col. 16, l. 49).

Claim 20:

Ranson teaches a number of the MSBs of the mask that are set to one is equal to the value of the control signal, with the remaining least significant bits ("LSBs") thereof set to zero (**Fig. 14, the least significant three bits of addend input 1403 are**

coupled to three-bit latch 1404. The twenty-nine most significant bits are coupled to ground). (Col. 15, l. 19 to col. 16, l. 49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 3, 8, 9, 12, 17, 18, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ranson et al.** (US-5887003), hereinafter Ranson.

Claims 3, 12 and 23:

The limitation "the control signal is three bits in length" is an obvious design choice and would be well within the ability of one skilled in the art to modify **Ranson** as to facilitate the selection of eight different inputs.

Claims 8, 9, 17, 18 and 22:

The limitation "the mask and the selected portion of the debug data are each S-bits in length, wherein S is equal to eight" is an obvious design choice and would be well within the ability of one skilled in the art to modify Ranson's state machine/counters control register circuitry 346 to load storage element 1204 (bit-wise mask) with different width mask data as to facilitate the masking of eight different inputs.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ohsawa (US-5644578) teaches inputting mask pattern data into inverted inputs of a plurality of AND gates with compared data in mask circuit 16 of Fig. 3. (reads on logic for zeroing in the claims).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JACQUES H. LOUIS JACQUES can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

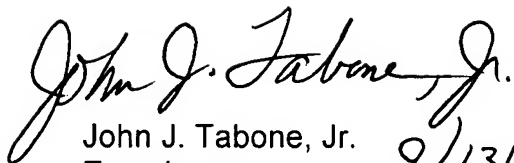
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/Cynthia Britt/
Primary Examiner
Art Unit 2117
9/13/07


John J. Tabone, Jr.
Examiner
Art Unit 2117 9/13/07